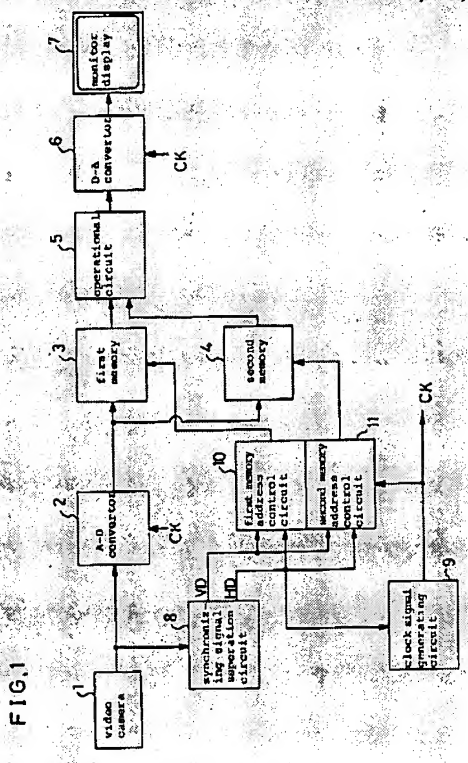

FIG. 1

[54] MAGNETIC MEDIUM PROCESSING APPARATUS

[75] Inventor: Kazuo Fukasawa, Yokohama, Japan

[73] Assignee: Kabushiki Kaisha Toshiba, Kawasaki, Japan

[21] Appl. No.: 306,958

[22] Filed: Sep. 16, 1994

[30] Foreign Application Priority Data

Sep. 16, 1993 [JP] Japan 5-229961
Aug. 2, 1994 [JP] Japan 6-181427

[51] Int. Cl.[6] G06K 7/08

[52] U.S. Cl. 235/449; 235/384; 235/475

[58] Field of Search 235/384, 449, 235/475

[56] References Cited

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FOREIGN PATENT DOCUMENTS

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Primary Examiner—John Sheppard
Assistant Examiner—Michael G. Lee
Attorney, Agent, or Firm—Cushman Darby & Cushman

[57] ABSTRACT

A magnetic medium processing apparatus includes a magnetism reading head for reading magnetic data recorded in a ticket, a peak value detector for detecting peak values of a signal output from the reading head, and a display for displaying the digital peak values detected by the peak value detector. Monitoring the state of reading by the reading head prevents unstable reading of magnetic data irrespective of whether the reading head is worn out.

13 Claims, 7 Drawing Sheets

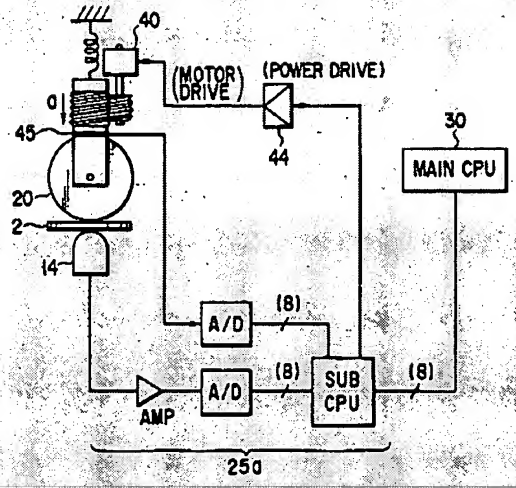


FIG. 1
(PRIOR ART)

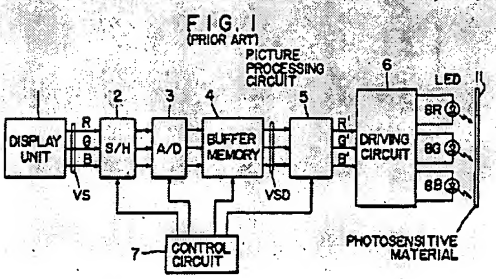


FIG. 2A
(PRIOR ART)

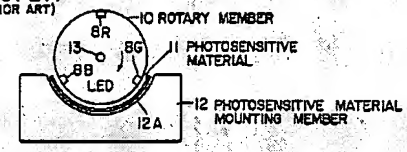
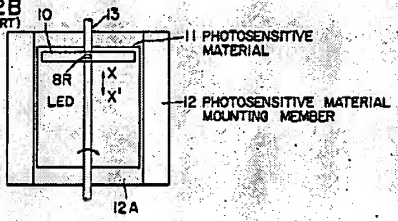


FIG. 2B
(PRIOR ART)



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57	US 20020137505		US-PGPU	20020926	37
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71	US 20010033734		US-PGPU	20011025	70
72	US 20010014165		US-PGPU	20010816	57
73	US 20010001598		US-PGPU	20010524	71
74	US 6737591 B1		USPAT	20040518	10
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DIGITAL TO ANALOG CONVERTER ARRAY

FIELD OF THE INVENTION

The present invention is related to the field of digital to analog converters, in one embodiment, for optical computing.

BACKGROUND OF THE INVENTION

Optical computing offers advantages over electronic computing for many applications. PCT publications WO 00/72104 and WO 00/73107 describe an optical analog computer which calculates general linear transforms using massively parallel processing. Applications include image compression, image enhancement, pattern recognition, signal identification, signal compression, optical interconnects and crossbar systems, morphologic operations, logical operations, image and signal transformation and modeling neural networks. While it may sometimes be possible, for example in image compression, to use input data that is initially in analog optical form, for many applications the input data is initially stored electronically in digital form, and must be converted into analog optical form before feeding it into the optical computer. To take advantage of the high computation speed of a massively parallel optical computer, there is a need for a system which rapidly converts a large amount of digital data into analog form.

Digital to analog converters (DAC) and analog to digital converters (ADC) are well known. An array of values can be converted from digital to analog form, or from analog to digital form, either in series, feeding each value into a single converter, or in parallel, simultaneously feeding all the values in the array into separate converters. For a very large array, serial conversion can be very slow, and parallel conversion can be very expensive since it requires a large number of converters.

Kleinfelder et al., "A 10 kframe/s 0.18 μm CMOS Digital Pixel Sensor with Pixel-Level Memory," 2001 IEEE International Solid-State Circuits Conference, Feb. 5–7, 2001, Session 6.1, CMOS Image Sensors with Embedded Processors, pages 68, 69 and 435, describe a system for parallel analog to digital conversion for a large array of pixels, in which the circuitry needed for each pixel is simpler and less expensive than a complete stand-alone analog to digital converter. A digital ramp signal, consisting of a sequence of 8-bit numbers in numerical order, is generated centrally, together with an analog ramp signal equivalent to the digital ramp signal, i.e. a triangle wave. Both signals are fed to all the pixels. Each pixel has a comparator circuit which compares the analog ramp signal to the value of the analog input for that pixel. When the ramp signal first exceeds the value of the analog input, the comparator circuit activates a digital latching circuit, which latches the current value of the digital ramp signal into the digital memory of that pixel. This digital memory serves as the digital output for the analog to digital conversion.

Albu et al., U.S. Pat. No. 6,320,565, describes a system for digital to analog conversion of a large array of pixels for driving an electro-optic display device, in which all the pixels in one row of the array are converted in parallel, followed by the next row, and continuing until the entire array is converted, then beginning a new frame. A global ramp generator generates an analog ramp signal going from zero to a maximum voltage, which is applied to capacitors associated with all the pixels in the row being processed at that time. An analog to digital converter produces a corresponding digital ramp signal. For each column in the array, there is a digital comparator which compares the digital ramp signal to an incoming digital video signal for the pixel at the intersection of that column and the row being processed. When the digital ramp signal matches the digital input signal for that column, a sample and hold circuit opens, and isolates the analog ramp signal from the capacitor associated with that pixel, and the voltage on that pixel then remains fixed, decaying slowly until the next frame is processed. In the next ramp cycle, the analog ramp signal is applied to the capacitors associated with the pixels in the next row, and so on. Several ramp cycles before a given row is processed, the analog ramp signal is temporarily reconnected to the capacitors of that row at a time when the analog ramp is close to zero, resetting those pixels to zero. This prevents image artifacts that would occur due to the residual state of the electro-optic material from previous frames.

SUMMARY OF THE INVENTION

An aspect of some embodiments of the invention concerns an array of circuitry for digital to analog conversion in parallel, in which signals for all the pixels of a two-dimensional array of pixels are converted simultaneously, rather than processing only one row of pixels at a time, as in Albu et al. Although this may require more complicated circuitry than Albu et al., for example possibly including a separate digital comparator for each pixel rather only one per column, it is possible to display a frame much more quickly than in the system disclosed by Albu et al. and the circuitry is still simpler and less expensive than a prior art array of circuitry with a stand alone digital to analog converter for each pixel. For the video display application of Albu et al., there would be no advantage to converting all of the pixels of a frame into analog form in parallel, since it is never necessary to display more than a few tens of frame per second, and converting all of the pixels in a frame in parallel would require more expensive hardware than only converting all of the pixels in a row in parallel. Even if only one row in the image is updated at a time, at tens of frames per second, it will appear to the human eye as if the entire image is changing continuously. For optical computing, however, it may be useful to convert thousands of frames per second from digital to analog form, for example to avoid having the processor remain idle for a large fraction of the time while the pixels are updated. Thus, for optical computing the cost of the additional hardware may be justified.

The circuitry in accordance with some embodiments of the invention accomplishes the reverse of the task accomplished by the analog to digital conversion array described by Kleinfelder et al. In an exemplary embodiment of the invention, there are a digital ramp signal and an equivalent analog ramp signal, which are optionally generated centrally, and are accessible to some or all of the elements of the array. In some embodiments of the invention, each element of the array comprises a digital comparator, which compares the digital ramp signal to the input value held in a digital memory associated with that element. When the two values are equal, the comparator generates an enabling signal which activates a sampling and holding circuit associated with that element. The sampling and holding circuit samples the value of the analog ramp signal at that time, and sets the value of an analog output for that element to the value of the analog ramp signal. The analog output is held at this value until the next time the comparator sends the enabling signal to the sampling and holding circuit. The sampling and holding circuit can be quite simple, optionally comprising only a transistor and a capacitor.

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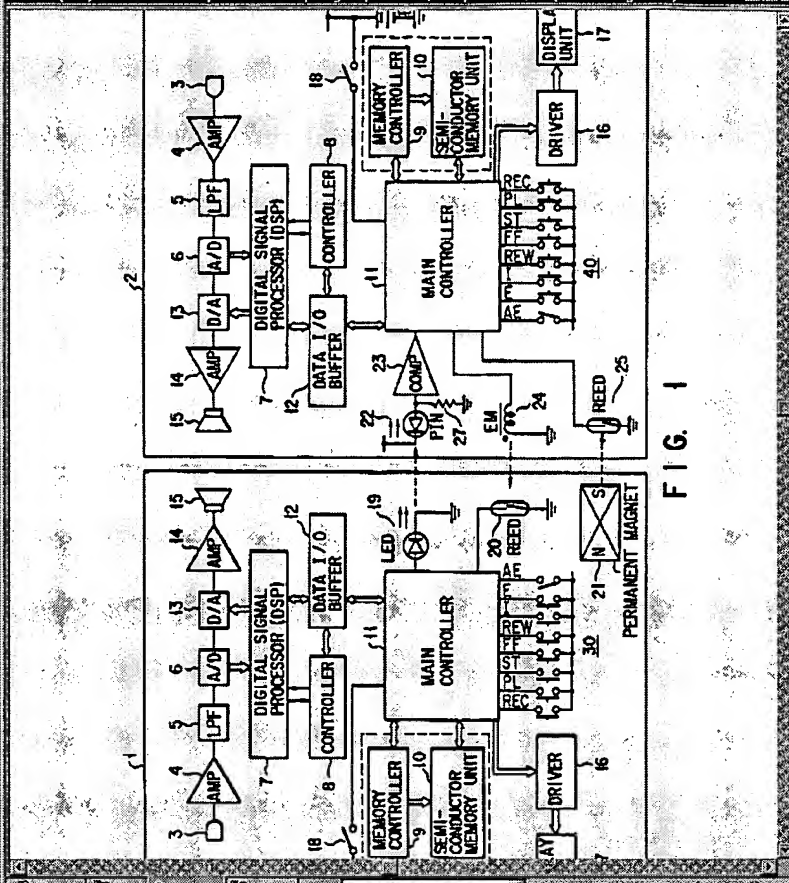

FIG. 1

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